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FIG. 1

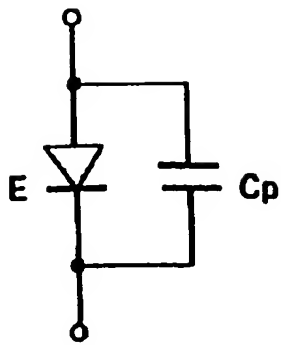


FIG. 2

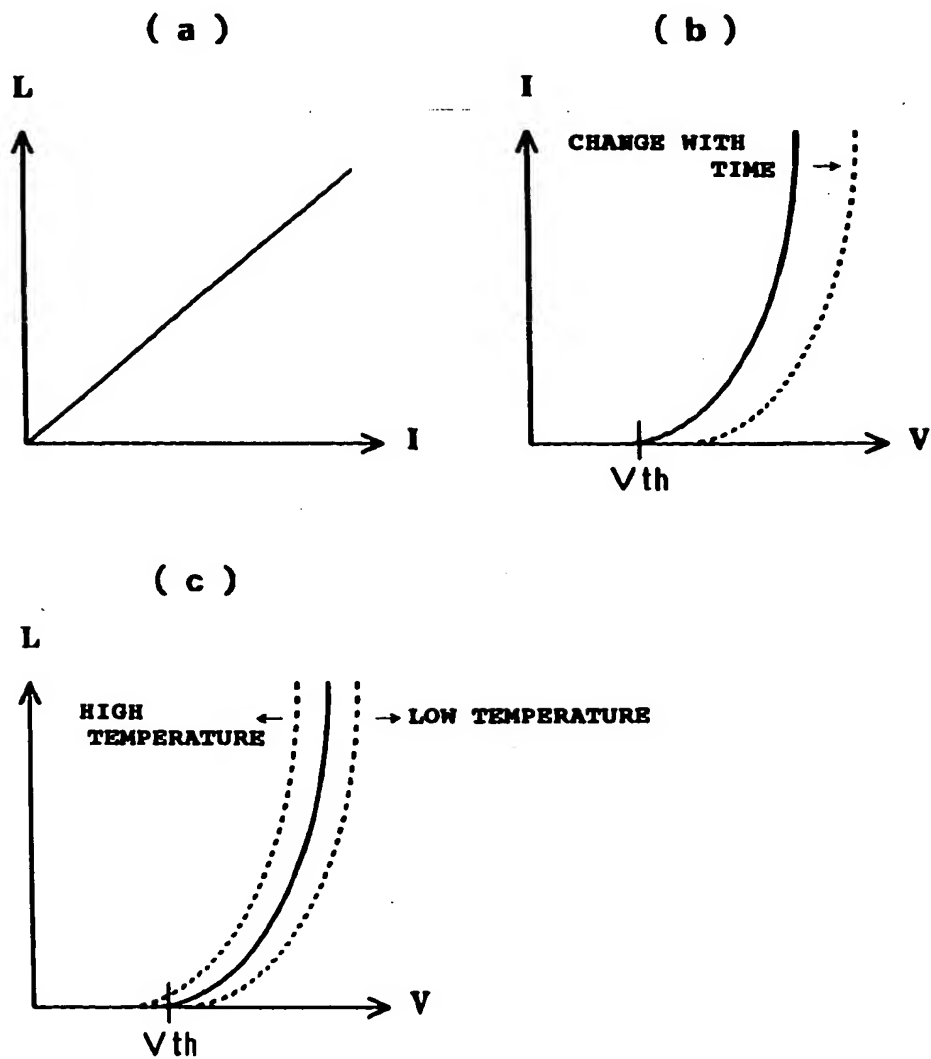


FIG. 3

FIG. 1 is a block diagram of a video display system. The system includes a **CONTROLLER** (15) which receives an **IMAGE SIGNAL** and an **INTENSITY CONTROL SIGNAL**. The controller is connected to a **SCAN DRIVER** (14) and a **DATA DRIVER** (13). The scan driver is connected to a pixel array (10) and provides a vertical clock signal (17) to the data driver. The data driver is connected to the pixel array and provides a horizontal clock signal (18) to a **S&H** (Sample and Hold) circuit (16). The S&H circuit is connected to a **VOLTAGE-CONTROL-SECTION** (18) and a **POWER SUPPLY-CIRCUIT** (17). The pixel array (10) consists of two rows of pixels, labeled 10A and 10B. Each pixel is connected to a horizontal line (n1, n2) and a vertical line (m1, m2). The pixel array is connected to a **DATA DRIVER** (13) and a **SCAN DRIVER** (14). The pixel array is also connected to a **VOLTAGE-CONTROL-SECTION** (18) and a **POWER SUPPLY-CIRCUIT** (17). The pixel array is connected to a **DATA DRIVER** (13) and a **SCAN DRIVER** (14). The pixel array is also connected to a **VOLTAGE-CONTROL-SECTION** (18) and a **POWER SUPPLY-CIRCUIT** (17).